What is claimed is:

1) A sputtered silicon structure being positioned on a work piece together with an operational circuitry and being formed on top of a sacrificial layer, said sputtered silicon structure having a thermal fabrication budget, said operational circuitry having a first critical thermal budget, wherein said thermal fabrication budget is smaller than said first critical thermal budget.

2) A sputtered silicon structure being formed on top of a sacrificial layer, said sputtered silicon structure having a thermal fabrication budget, said sacrificial layer having a second critical thermal budget, wherein said thermal fabrication budget is smaller than said second critical thermal budget.

3) The sputtered silicon structure of claim 1, wherein said sacrificial layer is made from a material dissolvable by a wet etchant.

4) The sputtered silicon structure of claim 3, wherein said wet etchant is selected from a group consisting of 6:1-20:1 buffered HF and $NH_4HF+HC_2H_3O_2+H_2O$.

5) The sputtered silicon structure of claim 4 having a first permeability rate that is up to ten times higher than a second wet etchant permeability rate of a comparable polysilicon structure.

6) The sputtered silicon structure of claim 1 or 2, wherein said sacrificial layer is made from a material dissolvable by a dry etchant.

7) The sputtered silicon structure of claim 6, wherein said material is an organic material.

8) The sputtered silicon structure of claim 7, wherein said organic material is polyimide.

9) The sputtered silicon structure of claim 1 or 2, wherein said sputtered silicon structure comprises a post-annealing configuration resulting from a pre-annealing configuration and a low temperature annealing transformation.

10) The sputtered silicon structure of claim 1, wherein said operational semiconductor circuitry includes an aluminum-metalization.

11) The sputtered silicon structure of claim 10, wherein said thermal fabrication budget is provided by a maximum annealing temperature of not more than 450° C.

12) The sputtered silicon structure of claim 1 or 2 being a released structure.

13) The sputtered silicon structure of claim 12, wherein said released structure has an

essentially buckling-free deformation configuration.

14) The sputtered silicon structure of claim 13 resulting from a sputtering with first sputtering criteria including:

A) an etchant selection; and

B) a sputtered structure thickness.

15) The sputtered silicon structure of claim 14, wherein said etchant selection is made from a group consisting of 6-20:1 buffered HF and $NH_4HF+HC_2H_3O_2+H_2O$.

16) The sputtered silicon structure of claim 13 having a variable sputtered layer thickness and a correlated curvature, wherein said correlated curvature essentially reduces with the square of an increase of the variable sputtered layer thickness for constant remaining first sputtering criteria.

17) The sputtered silicon structure of claim 12, wherein said released element has an essentially buckling-influenced deformation configuration.

18) The sputtered silicon structure of claim 17 resulting from a sputtering with second sputtering criteria including:

A) a sputtering power selection;

B) an ambient sputtering pressure selection;

C) a sacrificial layer material;

19) The sputtered silicon structure of claim 18, wherein said sputtering power selection is within a range of 1.5-2.5kW.

20) The sputtered silicon structure of claim 18, wherein said ambient sputtering pressure selection is within a range of 8-14mTorr argon.

21) The sputtered silicon structure of claim 18, wherein said sacrificial layer material is phosphosilicate glass.

22) The sputtered silicon structure of claim 18, wherein said sputtering power selection and said ambient sputtering pressure selection are zone-T type selections.

23) The annealed sputtered structure of claim 1 or 2, comprising at least one conductive layer combined with a core layer, said core layer having a first dissolving characteristic being compatible to a second dissolving characteristic of said at least one conductive layer.

24) The annealed sputtered structure of claim 23, wherein said core layer includes silicon and said conductive layer is sputtered from a material selected from a group consisting of TiW and TiN.

25) A sputtered silicon structure forming a cavity wall segment of a cavity within a work piece, said porous structure being accessible and permeable for a dissolving etchant capable of dissolving a cavity defining sacrificial layer.

26) The sputtered silicon structure of claim 25, wherein said annealed sputtered structure further comprises a sealing coating.

27) The annealed sputtered structure of claim 26, wherein said sealing coating comprises Si_3N_4.

28) A method of making a released sputtered silicon structure positioned on a work piece together with a electronic circuitry having a critical thermal budget, said method comprising the steps of:

A) assigning a deformation configuration to an intended structure theoretically representing said released sputtered structure;

B) selecting sputtering criteria according to said deformation configuration assigning;

C) providing a sacrificial layer;

D) sputtering a sputtered layer on top of said sacrificial layer;

E) shaping a structure from said sputtered layer; and

F) releasing said shaped structure by dissolving said sacrificial layer.

29) The method of claim 28, further comprising the step of transforming said sputtered layer from a pre-annealing configuration into a post-annealing configuration by applying a low temperature annealing process to said work piece, said low temperature annealing process having a thermal annealing budget smaller than said critical thermal budget.

30) The method of claim 29, whereby said low temperature annealing process has a maximum temperature of 450°C and said electronic circuitry includes an aluminum-metalization.

31) The method of claim 28, whereby said deformation configuration is an essentially buckling-free deformation configuration.

32) The method of claim 31, whereby said selecting includes:

A) selecting an etchant; and

B) selecting a thickness for said sputtered layer.

33) The method of claim 32, whereby said etching solvent is selected from a group consisting of 6-20:1 buffered HF and $NH_4HF+HC_2H_3O_2+H_2O$ for a sputtered layer including silicon.

34) The method of claim 28, whereby said deformation configuration is a buckling-influenced deformation configuration.

35) The method of claim 34, whereby said selecting includes:

A) selecting a sputtering power;

B) selecting an ambient sputtering pressure;

C) selecting a material for said sacrificial layer;

36) The method of claim 35, whereby said sputtering power is selected between 1.5 and 2.5kW for a sputtered layer including silicon.

37) The method of claim 35, whereby said ambient sputtering pressure is selected between 8 and 14mTorr argon for a sputtered layer including silicon.

38) The method of claim 35, whereby said sacrificial layer material is selected from phosphosilicate glass for a sputtered layer including silicon.

39) The method of claim 35, whereby said sputtering power and said ambient sputtering pressure are selected from a zone-T.

40) The method of claim 28, whereby said sputtered layer comprises a core silicon layer and at least one conductive layer combined with said core silicon layer, said core silicon layer having a first dissolving characteristic compatible with a second dissolving characteristic of said conductive layer.

41) The method of claim 40, whereby said conductive layer is made from a material selected from a group consisting of TiW and TiN.